Controlling the Output Voltage of a Step Up-Down Five-Level Inverter

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Abstract— The increasing demand for electrical energy must be balanced with using renewable energy. However, the use of renewable energy requires a system to maximize the conversion of renewable energy into electrical energy. Various topologies have been studied to achieve maximum energy conversion. Two types of inverters, namely step up-down, have been widely used but have their respective limitations. Step-down inverters can only be used in lower output voltage than input voltage conditions with simple control, while step-up inverters can only operate in higher output voltage than input voltage conditions. This paper aims to combine these two converters to have both step-up-down voltage functions, with the goal of expanding the operating range and maintaining the advantages of each type. Thus, a topology called a step-up-down five-level inverter with a simple voltage-controlled capacitor balancing system is proposed in this paper. Finally, the simulation and laboratory tests were done. This inverter operates in step-up-down voltage, and the voltage in capacitors is always balanced to reach the desired level. The voltage control was done to get the constant voltage event the load was changed.

Keywords— inverter; step up-down voltage; voltage balancer; voltage control

I. INTRODUCTION

In addition to the needs in the household, office, and industrial sectors, the present demand for electrical energy is constantly rising [1]. Furthermore, there are worries about fuel prices increasing, leading to extensive research and study on alternative energy [2]. Power plants using renewable energy sources have been the subject of organized and extensive research as an alternative energy source [3]. The utilization of renewable energy faces challenges in its application because the energy is produced in intermittent conditions, such as solar energy, and wind energy. The output voltage is described above as being in the form of direct voltage, hence they require a power conversion device that can change the output into an alternating current with an excellent level of efficiency.

Some scientists are conducting research on inverters, such as step-down, step-up, and step-up-down inverters, by concentrating basically on increasing conversion power without considering its flexibility. The multilevel inverter type, for instance, is a development of the traditional inverter topology. The waveform quality, harmonic distortion in the output current and voltage, increased power output, high voltage capacity, and low electromagnetic compatibility [4]–[7] are just a few benefits of this progress. There are some restrictions on various multilevel inverter designs, including cascade H-Bridge, flying capacitor, and neutral point clamped [8], [9]. Its restrictions are as follows: Unbalanced capacitor voltages are present in the flying capacitor and neutral point clamped topologies, and multiple isolated DC sources are needed for the cascaded H-Bridge architecture [10], [11]. The limitations of conventional multilevel inverters have been investigated in several studies [12], [13]. In these studies, reduced control is used to make the inverter less complicated while still operating as a step-down inverter most of the time.

The step-up inverter was discussed by other researchers [14]. With only one source needed, this design can provide output that is more than the input. This sort of inverter's limitation to step-up voltage circumstances makes it a drawback. A step up-down inverter was created to address this issue [15]. The system is implemented as a mix of DC-DC converters and H-Bridge inverters, which call for a few dc-link capacitors and have an impact on efficiency values [16]–[18]. A single-stage step up-down inverter approach was integrated in a further study [17] employing fewer components at a lower cost [19], [20]. An output voltage regulation system is required for renewable energy applications where the voltage must be maintained constant. This study aims to propose solutions for inverters that are described above using a combination of five-level inverters that can function as a step up-down on the output voltage side. Two capacitors in the proposed five-level inverter are always operated in balance condition, and on the output side, a voltage regulation device can be installed to maintain the output voltage. As a result, this inverter will have a wide operation range and be appropriate for applications involving renewable energy. The proposed power electronic switches will be fewer than those made by researchers [7], [12], and [13], which will have simpler implications for the control circuit.

In the second section, a method of operations and output voltage regulation approach were explained. The results and analysis regarding the simulated and implemented step up-down inverter are completed in the third section, In the end of the section was concluded.

II. METHOD

As illustrated in Figure 1, the proposed power circuit is made up of two main components: a step-up and step-down converter and a five-level inverter with a voltage balancer on the capacitor. Two power switches S1 and S2 and two capacitors C1 and C2 that serve as an input voltage divider are

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present in the inverter's five-level element. The H-bridge inverter, which generates the output voltage polarity, is integrated into this circuit. Therefore, the output voltage of these five levels will always function as a five-level step down inverter.

The proposed topology is more effective since it has a wider operating range because the output of the five-level inverter is connected to a step up-down converter that works to increase or decrease the voltage. The basic idea behind controlling capacitor voltage balance is to ensure that the middle charge is charged and discharged in the capacitor in a balanced manner throughout operation.

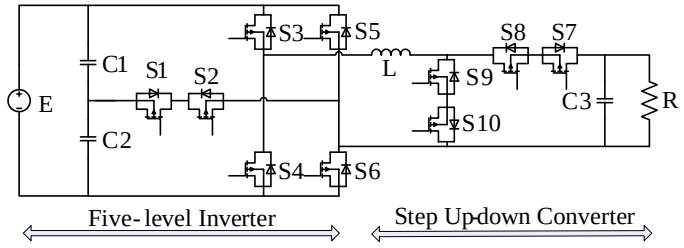


Figure 1. Five-level inverter step up-down type.

A. Step Down Mode

The procedure in step-down mode goes through tree steps on a half positive cycle and three steps on negative cycle:

1. Current flows from the DC source to the inductor (L) during the first cycle when the power switches S3 and S6 are switched on. The load is receiving current because the power switch S8 is turned on. The output voltage is E.
2. The current flows from the DC source to the inductor (L) since the power switch S3 is active during the second cycle, and then to the load because the power switch S8 is active before returning through switch S1. This condition makes the capacitor C2 charge before it returns to the DC source. The output voltage is E/2.
3. The third cycle, which can occur in both positive and negative cycles, was called a free-wheeling scenario. Power switches S6, and S8 are active on the positive cycle,
4. The current flows from the DC source to the load during the fourth cycle of operation, then through the active power switch S5 to the inductor (L), before returning to the DC source via switch S4. The output voltage is -E.
5. The sixth cycle, the capacitor C1 charges when the current flows from the DC source to the inductor (L) via S2, the load switches S7 and go back to the DC source via S4. The output voltage is -E/2.
6. The fifth cycle, which can occur in both positive and negative cycles, was called a free-wheeling scenario. Power switches S4, and S7 are active on the negative cycle.

The six cycles will always be repeated indefinitely. Whereas power switches S1, S2, S5, and S6 operated at high frequency, power switches S9 and S10 are always idle. On positive and negative cycles, power switches S3 and S4 will always work at 50 Hz. The second and fifth procedure control the voltage to balance the voltage across the capacitor in a very basic method. The voltage across the capacitor (C1 and C2) will be charged and discharged in this condition. Table I summarizes the switching logic and output voltage in the step down operating mode. The voltage balance across capacitors C1 and C2 will always be maintained properly with this technique.

TABLE I. LOGIC SIGNAL OF POWER SWITCH ON STEP DOWN MODE

S1	S2	S3	S4	S5	S6	S7	S8	Vo
Off	Off	**On**	Off	Off	**On**	Off	**On**	**E**
On	Off	**On**	Off	Off	Off	Off	**On**	**½ E**
Off	Off	Off	Off	Off	**ON**	Off	**On**	**0**
Off	Off	Off	**On**	**On**	Off	**On**	Off	**-E**
Off	**On**	Off	**On**	Off	Off	**On**	Off	**-½ E**
Off	Off	Off	**On**	Off	Off	**On**	Off	**0**

B. Step Up Mode

The procedure in step-up mode goes through five steps on a half positive cycle:

1. The goal of the first cycle is to short-circuit the inductor so that the voltage across it equals the input voltage. The power switches S3, S9, and S6 are all active in this state.
2. The voltage on the inductor, along with the input voltage, will be pushed towards the load during the second cycle, requiring the power switches S3, S8, S6 to be active. The output voltage will be greater than the input voltage if the first and second conditions are completed.
3. The goal of the third cycle is to short-circuit the inductor so that the voltage across it equals a half input voltage. The power switches S3, S9, and S1 are all active in this state.
4. The voltage on the inductor, along with a half input voltage, will be pushed towards the load during the second cycle, requiring the power switches S3, S8, S1 to be active. The output voltage will be greater than a half input voltage if the third and fourth conditions are completed.
5. The fifth cycle, which can occur in both positive and negative cycles, was called a free-wheeling scenario. Power switches S8, and S10 are active on the positive cycle, and switches S9, and S7 are active on the negative cycle.

Table II summarizes the switching logic and output voltage in the step-up operating mode on a half positive cycle. The third and fourth procedure control the voltage to balance the voltage across the capacitor (C2) in a half positive cycle. Table III summarizes the switching logic and output voltage in the step-up operating mode on a half negative cycle. The eighth and sixth procedure control the voltage to balance the voltage across the capacitor (C1) in a half negative cycle.

TABLE II. LOGIC SIGNAL OF POWER SWITCH ON A HALF POSITIVE CYCLE STEP UP MODE

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	Condition
Off	Off	**On**	Off	Off	**On**	Off	Off	**On**	Off	$\mathbf{V_L = E}$
Off	Off	**On**	Off	Off	**On**	Off	**On**	Off	Off	$\mathbf{V_o \geq E}$
On	Off	**On**	Off	Off	Off	Off	Off	**On**	Off	$\mathbf{V_L = ½ E}$
On	Off	**On**	Off	Off	Off	Off	**On**	Off	Off	$\mathbf{V_L \geq ½ E}$
Off	Off	Off	**Off**	Off	Off	Off	**On**	Off	**On**	Freewheeling

TABLE III. LOGIC SIGNAL OF POWER SWITCH ON A HALF NEGATIVE CYCLE STEP UP MODE

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	Condition
Off	Off	Off	**On**	**On**	Off	Off	Off	Off	**On**	$\mathbf{V_L = -E}$
Off	Off	Off	**On**	**On**	Off	Off	**On**	Off	Off	$\mathbf{V_o \geq -E}$
Off	**On**	Off	**On**	Off	**Off**	Off	Off	**On**	Off	$\mathbf{V_L = -½\ E}$
Off	**On**	Off	**On**	Off	Off	Off	**On**	Off	Off	$\mathbf{V_L \geq - ½\ E}$
Off	Off	Off	Off	Off	Off	**On**	Off	**On**	Off	Freewheeling

Based on the operating mode of step up or step down, it can be seen that the voltage across the capacitor is constantly charging and discharging, implying that the voltage across the capacitor will be constant with this approach. Thus, the five-level concept for balancing the voltage across the capacitor will work well.

C. Voltage Control Strategy

The step up-down inverter that has been studied is an inverter whose output voltage is controlled, where the control used is a proportional integral (PI) type with the goal: the output voltage remains stable even when the load changes, as shown in (1).

$$U(s) = Kp\ (1 + \frac{1}{Tis}) \quad (1)$$

Where K_p is a gain proportional, T_{is} is K_p/Ki (Gain PI controller) and K_i is Gain integral. The step-up-down inverter is controlled in two parts: the five-level inverter section is controlled by operating the power switches S1, S2, S3, S4, S5, and S6, and the step-down section of the converter is controlled by operating the power switches S7, S8, S9, and S10. Control is carried out on the output voltage side of the sensor using the controls outlined above. Figure 2 depicts the proposed scheme, which has been thoroughly researched.

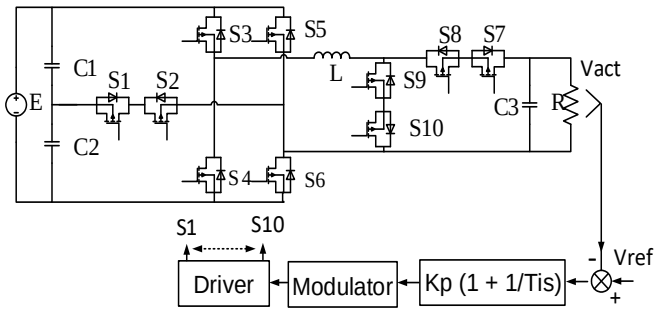


Figure 2. The step-up-down inverter-controlled voltage scheme

The process of control begins with the Vo output, which is recognized by the main sensor (named Vact). The reference voltage (Vref) is compared with Vact to determine the error value, as shown in (2). The modulator will modulate the PI control input to activate the power switches based on the error value.

$$e(s) = Vo\ (s) - Vref\ (s) \quad (2)$$

The modulation mechanism is carried out by comparing the PI control output to the multilevel carrier signal, resulting in a pulse width modulation output (PWM). This signal is utilized to control the power switches S1, S6, S2, and S4 on the inverter side, which operate at high frequency to form five levels. While the gating signal for switches S4 and S3 is derived by comparing the sinusoidal voltage (Vsin) taken from the Vref voltage to zero. According to the reference frequency, the output signal is a zero crossing with a frequency of 50 Hz. Vsin is also used for controlling the step up-down converter, which is done by comparing the Vsin value to zero. The output signal is modified using a sequence of logic gates working together with the PWM created in the first process. Using this concept, the step up-down inverter's output voltage will always be effectively maintained even if the load on the output side changes; this can be seen by comparing the output voltage, which will always follow the reference voltage. Figure 3 depicts the program algorithm from Figure 2's control scheme.

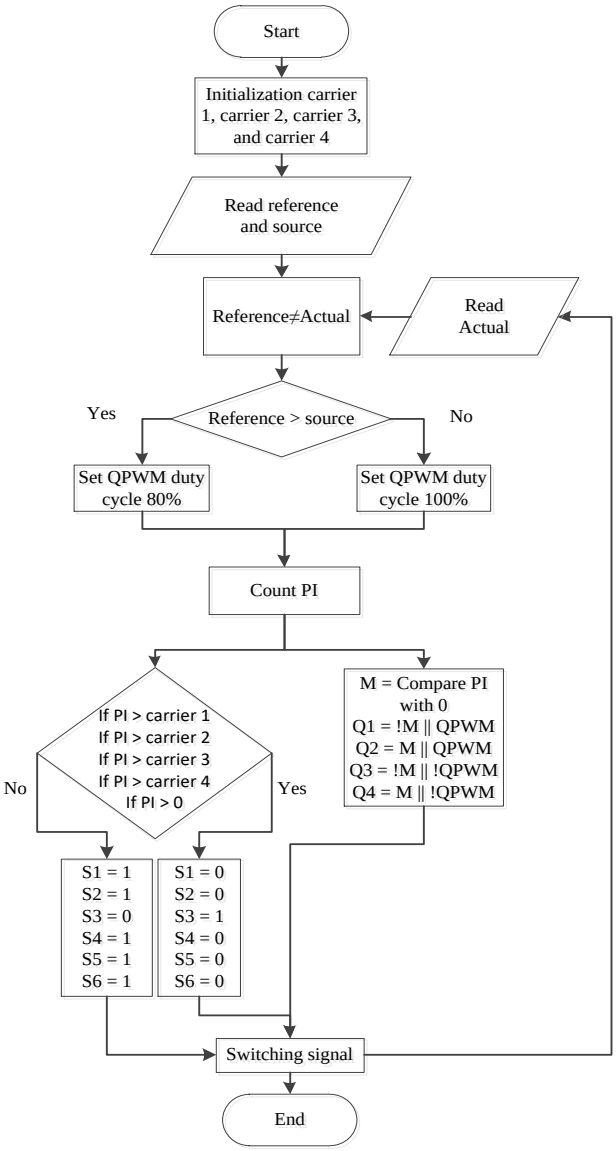


Figure 3. Program algorithm

D. Components and Parameters

This work was validated using the same parameters and components in two ways: computer-generated simulation and laboratory the application is submitted. The components are chosen through a comparison of the simulation results to the components that are commonly available, so that these may be obtained more easily during implementation. The load value (resistor) must be considered because, in addition to the load value, the power value must be kept contemplated so that resistance is always maintained properly. The value of the

inductor is determined based on the simulation value and the current that happens during the simulation with the goal to determine the value of the quantity of wire utilized. This inductance is then confirmed using an inductor meter set to the frequency in Table V. The C1 and C2 have identical values to maintain a balance of charging and discharging voltage, which is always maintained during the process of generating the applied level. The value of C3 is used to reduce the harmonics of the output voltage, and it should be noted that the output voltage is in the form of AC voltage, so the C3 value must be adjusted to the market value of the components. Table IV and Table V indicate the components and parameters used in the simulation.

TABLE IV. COMPONENTS

Components	Type
Microntroller	STM32F407
Power MOSFET	IRFP250
Voltage Sensor	HX10-P
Current Sensor	LV25-P
Optocoupler	TLP250

TABLE V. SIMULATION PARAMETERS

Components	Value
DC Source	20V
Capacitor C1 dan C2	470µF
Capacitor C3	1uF
Inductor	5mH
Load	100 - 50 Ω
Gain Proportional	0.03
Gain Integral	0.001
Switching Frequency	10KHz

III. RESULTS AND DISCUSSION

Figure 4 displays the final result of hardware implementation in the laboratory; all parameters implemented are in accordance with Table IV and Table V.

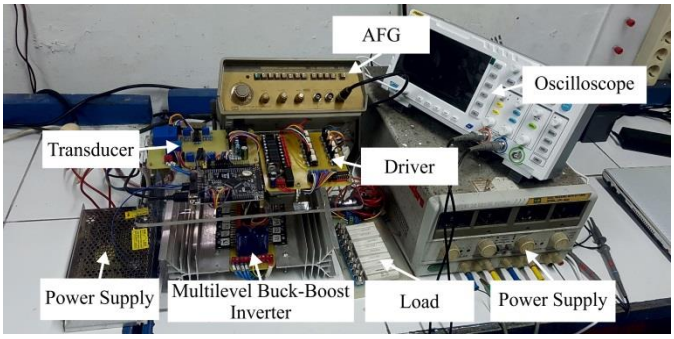
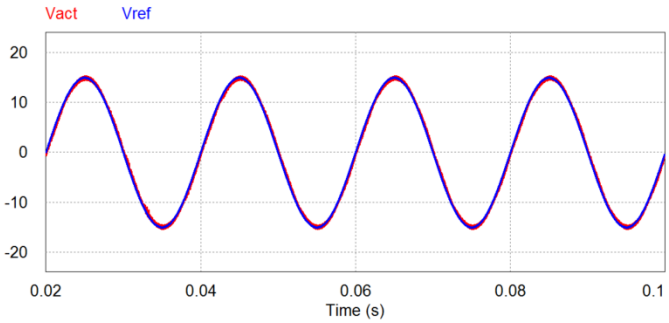


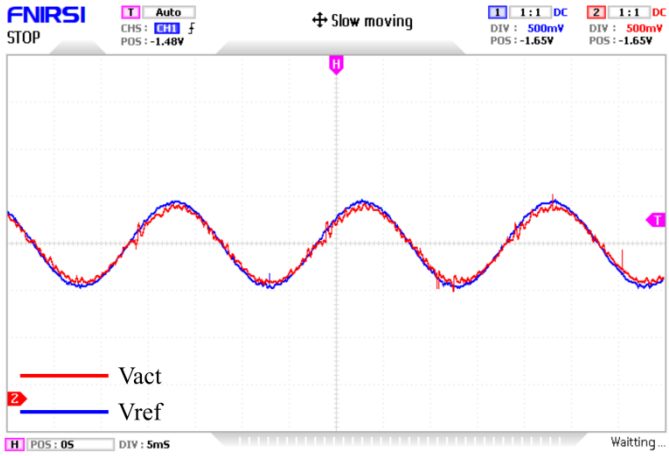
Figure 4. Hardware implementation

The results of testing on computational and hardware simulations in step down settings, with the oscilloscope probe set 10 times the gain are shown in the implementation figure. During computational simulations, it can be seen that the actual voltage (Vact) consistently complies with the reference voltage (Vref), allowing the output voltage control method to be appropriately maintained with already established parameters, as shown in Figure 5(a). In the implementation, the actual voltage (Vact) constantly matches the reference voltage (Vref), as shown in Figure 5(b). It is possible to establish that there is a match between computational simulation and implementation by comparing Figures 5(a) and 5(b).

Considering the inverter topology applied is five levels, the output side of the five-level inverter is the next stage of testing. As can be seen in Figure 6(a), which was executed during a computational simulation and Figure 6(b), which was achieved during laboratory testing, the magnitude of the voltage at each level was +20 V, +10 V, 0V, -10V, -20V.

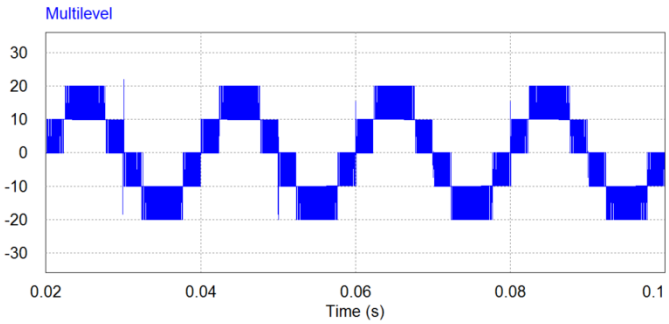


(a)

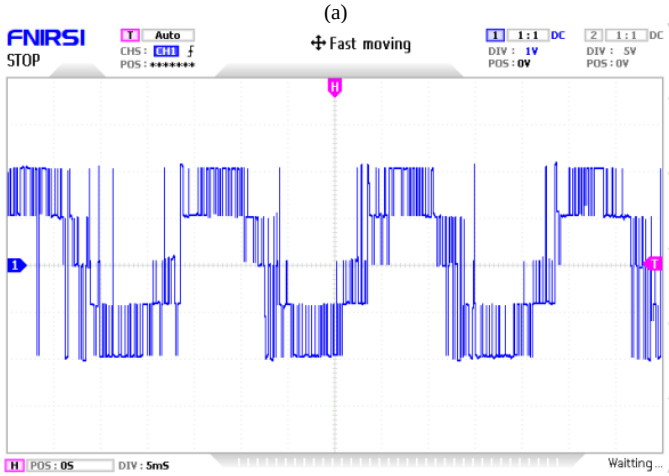


(b)

Figure 5. Vact and Vref under buck conditions: (a) Simulation and (b) Implementation



(a)

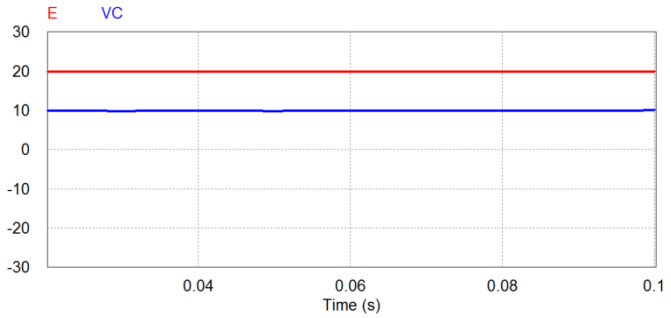


(b)

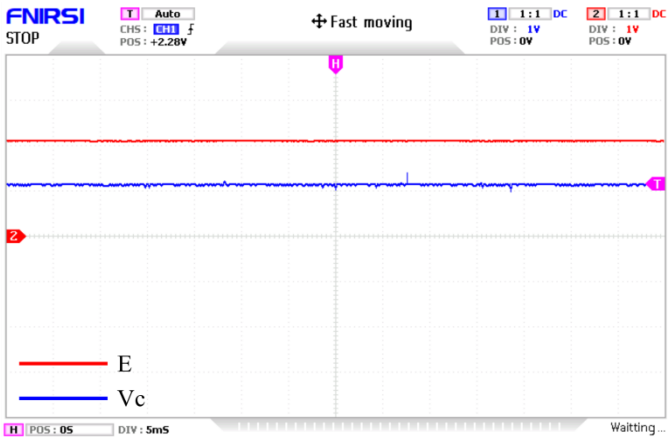
Figure 6. Five-level inverter output waveform under buck conditions: (a) Simulation and (b) Implementation

These voltage levels will be correctly configured if there is a voltage balance between the two capacitors (C1 and C2),

which indicates that the processes of charging and discharging the capacitors can be carried out during the inverter's working cycle. To ensure further measurements at the voltage of each capacitor (C1 and C2) are done. As illustrated in Figure 7, a voltage of 10 V (1/2 E) exists in each capacitor in both computational and implementation simulations.

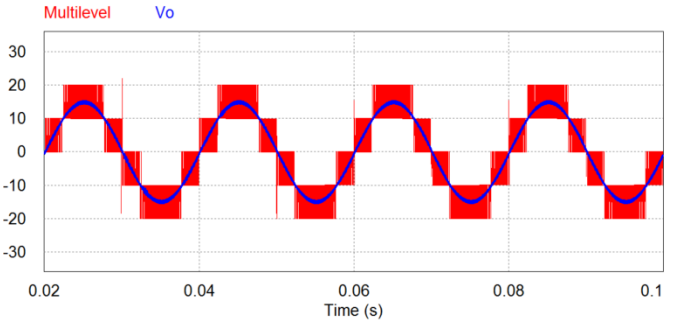


(a)

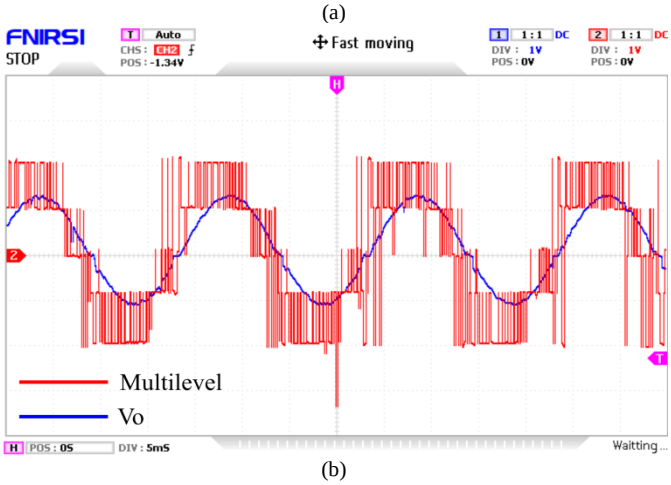


(b)

Figure 7. Voltage on capacitor under buck conditions: (a) Simulation and (b) Implementation



(a)



(b)

Figure 8. Five-level inverter and fundamental voltage under buck conditions: (a) Simulation and (b) Implementation

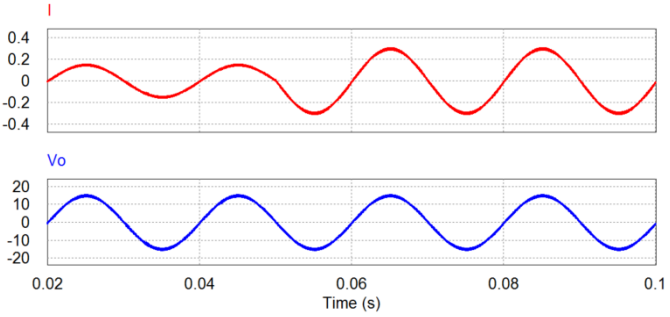
Figure 8 depicts the output of a five-level inverter and its basic value (sinusoidal wave). The observed results demonstrate a correlation between the results of computational simulations and implementation. This inverter has been programmed to step down, and the output voltage is lower than the input source voltage. It is clear that both the simulation and implementation results of the tool function under buck conditions, with the output voltage of 15V being less than the source voltage.

A changing load test is used to verify the last stage of the step down inverter. The current on the output side changes when the load changes although the voltage on the output voltage side remains stable when the load changes, as shown in Figure 9.

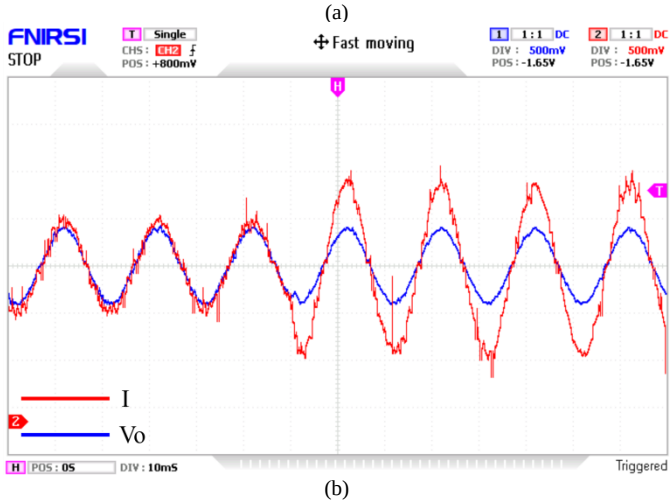
The step up inverter test is performed after the step down inverter test has been successfully completed. The step up inverter test is carried out by increasing the Vref value. Figure 10 shows that in both simulation and implementation, the Vact output voltage will constantly correspond to the reference voltage Vref.

The output voltage of the five-level inverter remains constant when working as a step-up, indicating that the specified design is functioning properly, as illustrated in Figure 11. Because the input voltage value is 20 V, this five-level inverter has the advantage of having a reduced power switch voltage stress of 10 V.

The voltage levels (five levels) could potentially be seen to be going properly, therefore the voltage on the capacitor will always be maintained, both charging and discharging. The voltage across the capacitor is determined after further testing, as shown in Figure 12, where the voltage across capacitors C1 and C2 is 10 V. Finally, by using both step-down and step-up operation modes with good charging and discharging, the voltage balance in the capacitor is always well maintained without the need for a complicated control system.



(a)



(b)

Figure 9. Current and voltage output waveform under buck conditions: (a) Simulation and (b) Implementation

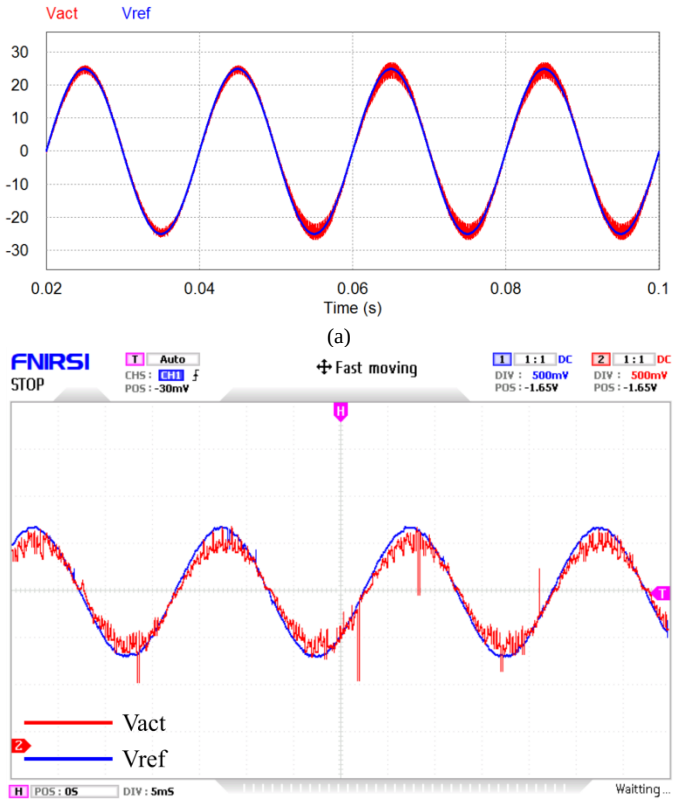


Figure 10. Vact and Vref under boost conditions: (a) Simulation and (b) Implementation

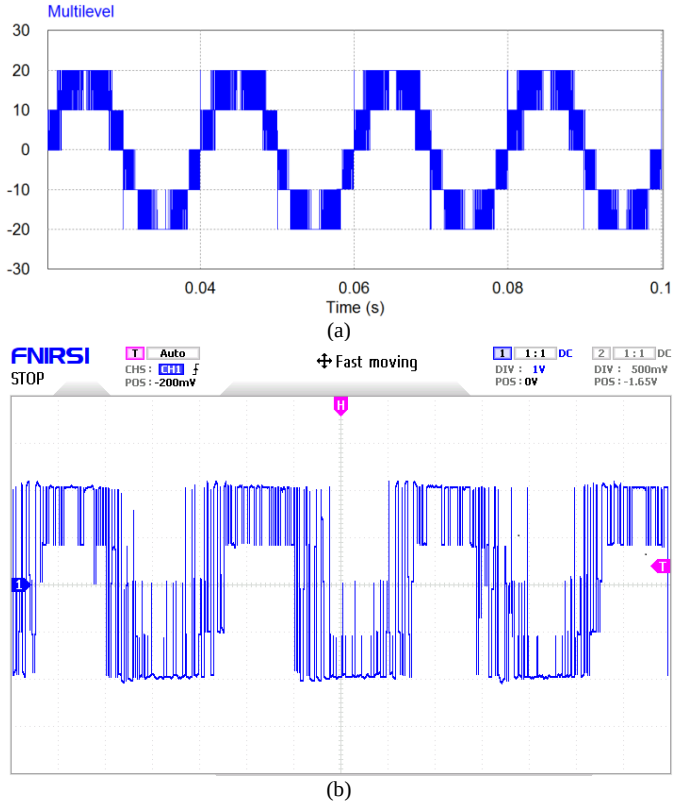


Figure 11. Five-level inverter output waveform under boost conditions: (a) Simulation and (b) Implementation

Figure 13 depicts a comparison of the five-level voltage with its fundamental value. The fundamental output voltage demonstrates that the voltage has an amplitude of 25 V more than the input voltage value of 20 V. Based on the results of this test, it appears that this step-up inverter is functional. When the findings of this study are compared to the findings of studies [7], [12], and [13], it appears that the strategy of balancing the voltage on the capacitor based on a basic mode of operation can create voltage in step up and step down situations.

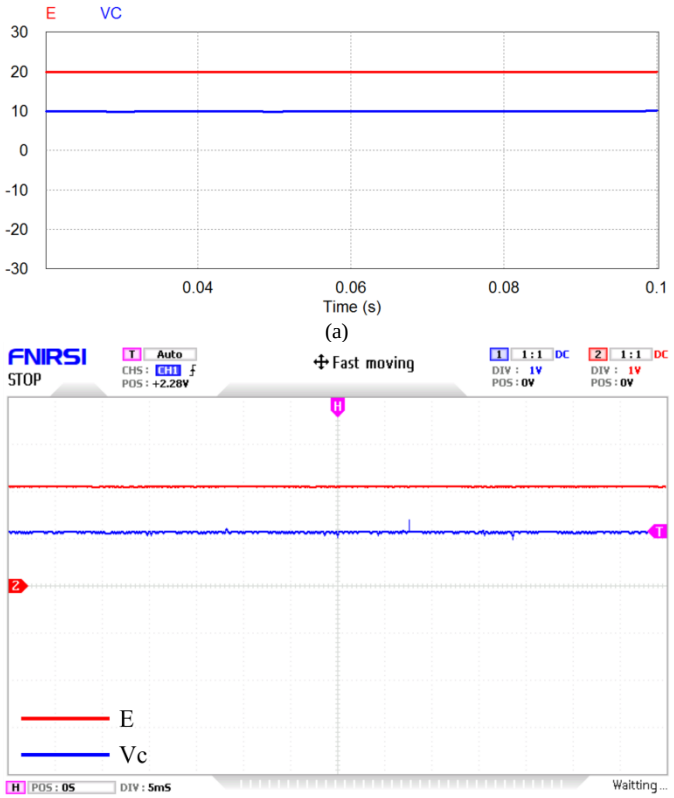


Figure 12. Voltage on capacitor under boost conditions: (a) Simulation and (b) Implementation

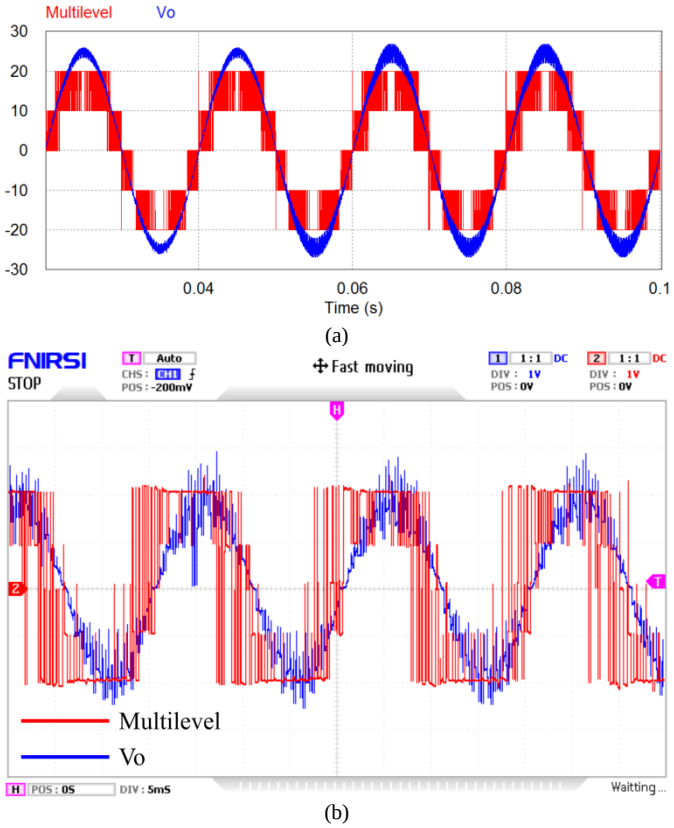


Figure 13. Five-level inverter and fundamental voltage under boost conditions: (a) Simulation and (b) Implementation

The final stage of this investigation included a load change test. Figure 14 shows that both the computational simulation

and the physical building of this step-up inverter are capable of maintaining a steady output voltage even when the load changes (the output current appears to change). In comparison to studies [17], load testing has not yet been performed, thus the reaction to changes in load must be examined further. The planned system can work properly and correctly based on the findings of extensive testing in both step up and step down scenarios with changes in load.

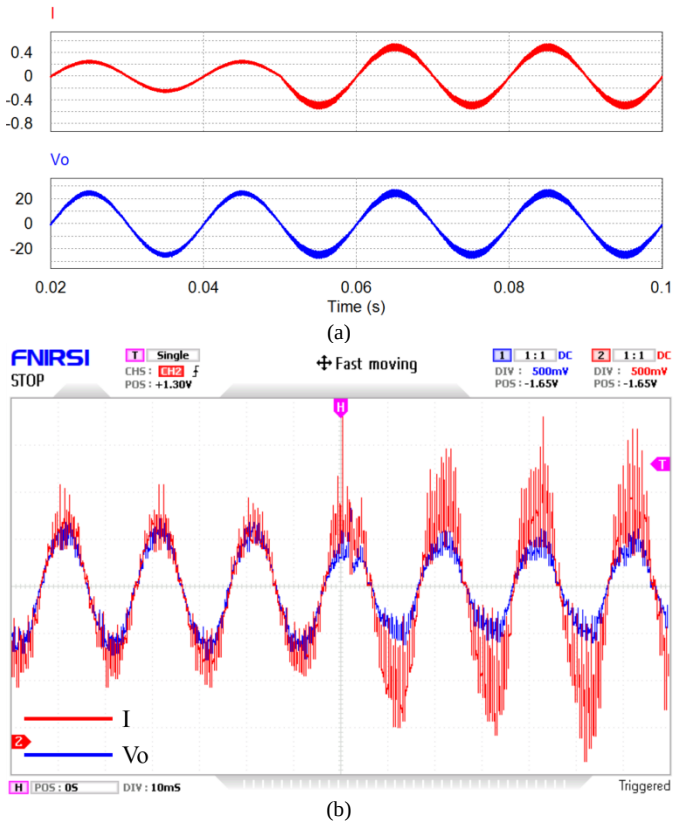


Figure 14. Current and voltage output waveform under boost conditions: (a) Simulation and (b) Implementation

IV. Conclusion

According to the results from the study, computational simulation, and laboratory implementation of the five-level step-up-down inverter type can be successful. Implementing an output voltage control technique ensures that the output voltage is always adequately maintained, even when the load changes. The capacitor's voltage balance can be maintained by using the charging and discharging operating modes in each step-up and step-down cycle. When this type of inverter is combined with a renewable energy source, such as photovoltaics, it creates a very good system since the output voltage can always be maintained constantly even when the load changes.

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